



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/772,590	02/04/2004	Roberto Pelliconi	61181-00011USPX	2338

32914 7590 11/28/2007
GARDERE WYNNE SEWELL LLP
INTELLECTUAL PROPERTY SECTION
3000 THANKSGIVING TOWER
1601 ELM ST
DALLAS, TX 75201-4761

EXAMINER

PUENTE, EVA YI ZHENG

ART UNIT	PAPER NUMBER
----------	--------------

2611

MAIL DATE	DELIVERY MODE
-----------	---------------

11/28/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/772,590	PELLICONI ET AL.	
	Examiner	Art Unit	
	Eva Y. Puente	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 September 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 2-12, 14-17, 19 and 21-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 2-12, 14-17, 19 and 21-25 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see Amendment, filed 9/4/07, with respect to the rejection(s) of claim(s) 2-12, 14-17, 19, and 21-25 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made.
2. Objection to drawing has been withdrawn.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 5 and 7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a) Regarding to claim 5, Recitation: "lower sampling period" is being indefinite and failed to particularly point out what is meant by lower sampling period.

b) Regarding to claim 7, recitation "lower than half the transmission period" is being indefinite and failed to particularly point out what is meant by lower transmission period.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 4, 8, and 22-24 are rejected under 35 U.S.C. 102(e) as being unpatentable by Hirose et al (US 6,917,995).

a) Regarding to claim 4, Hirose et al disclose a method for synchronizing a data interchange in a semiconductor substrate integrated electronic circuit (IC; abstract) comprising a transmitter block (block A in Fig. 1A) and a receiver block (block B in Fig. 1A) connected through a communication network, comprising:

generating a data signal having a transmission period on a first line that from said transmitter block must be received by the receiver block (command bus line in Fig. 1A);

generating on a second line a congestion signal from the receiver block to the transmitter block when a congestion event (when number of commands reach maximum limit) of the receiver block occurs in order to interrupt the transmission of said data signal (BUSY bus line in Fig. 1A; Col 1, L52-59); and

generating on a third line a synchro signal starting from said transmitter block (STRB bus line in Fig. 1A), this synchro signal indicating to the receiver block that the data signal comprises a new datum (Fig. 1B; Col 1, L60-65), and in that the congestion

signal interrupts also the transmission of said synchro signal when a congestion event of the receiver block occurs (Fig. 1B; Col 1, L63-Col 2, L6; STRB signal stops after the BUSY signal is sent); and

reading, by the receiver block, of the data signal with a different sampling period from the transmission period of the transmitter block (device A and device B are generated with different clock signals).

a) Regarding to claim 8, Hirose et al disclose a method for synchronizing a data interchange in a semiconductor substrate integrated electronic circuit (IC; abstract) comprising a transmitter block (block A in Fig. 1A) and a receiver block (block B in Fig. 1A) connected through a communication network, comprising:

generating a data signal having a transmission period on a first line that from said transmitter block must be received by the receiver block (command bus line in Fig. 1A);

generating on a second line a congestion signal from the receiver block to the transmitter block when a congestion event (when number of commands reach maximum limit) of the receiver block occurs in order to interrupt the transmission of said data signal (BUSY bus line in Fig. 1A; Col 1, L52-59); and

generating on a third line a synchro signal starting from said transmitter block (STRB bus line in Fig. 1A), this synchro signal indicating to the receiver block that the data signal comprises a new datum (Fig. 1B; Col 1, L60-65), and in that the congestion signal interrupts also the transmission of said synchro signal when a congestion event of the receiver block occurs (Fig. 1B; Col 1, L63-Col 2, L6; STRB signal stops after the BUSY signal is sent); and

generating, on a couple of further line, a couple of unidirectional signals indicating the transmission direction between said transmitter block and said receiver block (Fig. 2A and 2C), a negotiation to define the transmission direction being controlled by a further transmission request signal driven by the receiver block (counter 18, controller A, counter 18B, controller B constitutes as negotiator).

c) Regarding to claim 22, Hirose et al disclose a communication system, comprising:

- a first communication block (block A in Fig. 1A);

- a second communication block (block B in Fig. 1A);

- a communication network interconnecting the first and second communication blocks (Fig. 1A); the communication network comprising:

 - a first communication line for carrying a data signal (command bus line in Fig. 1A);

 - a second communication line for carrying a congestion signal (BUSY bus line in Fig. 1A; Col 1, L52-59); and

 - a third communication line for carrying a synchronization signal (STRB bus line in Fig. 1A); wherein the synchronization signal is active whenever the data signal on the first communication is new datum and inactive whenever the congestion signal on the second communication line is active (Fig. 1B; STRB signal is active as the command signal is new and within process limit, while STRB stops transmitting when BUSY is active after limit of commands has reached);

wherein the first, second and third communication lines are bi-directional, further including:

a transmit signal line (CMD_READY_A in Fig. 2C); and

a receive signal line (CMD_READY_B in Fig. 2C);

wherein the transmit and receiver signal lines interconnected the first and second communication blocks (block A and B), and control signals thereon specify which of the first and second communication blocks is a transmitter of the data signal and which of the first and second communication blocks is a receiver of the data signal (counter 18, controller A, counter 18B, controller B constitutes as negotiator).

d) Regarding to claim 23, Hirose et al disclose a request signal line that interconnects the first and second communication blocks (CMD_STRB_A in Fig. 2C), and a control signal thereon used to negotiate which of the first and second communication blocks is to be transmitter/receiver (13A and 13B; counter 18, controller A, counter 18B, controller B in Fig. 2C).

e) Regarding to claim 24, Hirose et al disclose a communication system, comprising:

a first communication block (block A in Fig. 1A);

a second communication block (block B in Fig. 1A);

a communication network interconnecting the first and second communication blocks (Fig. 1A); the communication network comprising:

a first communication line for carrying a data signal (command bus line in Fig. 1A);

a second communication line for carrying a congestion signal (BUSY bus line in Fig. 1A; Col 1, L52-59); and

a third communication line for carrying a synchronization signal (STRB bus line in Fig. 1A); wherein the synchronization signal is active whenever the data signal on the first communication is new datum and inactive whenever the congestion signal on the second communication line is active (Fig. 1B; STRB signal is active as the command signal is new and within process limit, while STRB stops transmitting when BUSY is active after limit of commands has reached);

wherein transmission of the data signal in the first communication line is inhibited whenever the congestion signal on the second communication line is active (Fig. 1B; command signal is stop after 5 commands, while BUSY signal is active after the 5 commands).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 2, 3, 14-17, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirose et al (US 6,917,995) in view of Dabral (US 2004/0044919).

a) Regarding to claim 2, Hirose et al disclose a method for synchronizing a data interchange in a semiconductor substrate integrated electronic circuit (IC; abstract)

comprising a transmitter block (block A in Fig. 1A) and a receiver block (block B in Fig. 1A) connected through a communication network, comprising:

generating a data signal having a transmission period on a first line that from said transmitter block must be received by the receiver block (command bus line in Fig. 1A);

generating on a second line a congestion signal from the receiver block to the transmitter block when a congestion event (when number of commands reach maximum limit) of the receiver block occurs in order to interrupt the transmission of said data signal (BUSY bus line in Fig. 1A; Col 1, L52-59); and

generating on a third line a synchro signal starting from said transmitter block (STRB bus line in Fig. 1A), this synchro signal indicating to the receiver block that the data signal comprises a new datum (Fig. 1B; Col 1, L60-65), and in that the congestion signal interrupts also the transmission of said synchro signal when a congestion event of the receiver block occurs (Fig. 1B; Col 1, L63-Col 2, L6; STRB signal stops after the BUSY signal is sent).

Hirose et al disclose all the subject matter above except is silent about whether or not the synchro signal is delayed with respect to the data signal. However, Dabral, in the same field of endeavor, disclose a data transfer system between two devices, wherein the strobe signals are delayed (15 in Fig. 1) before transmitting data to latches 13 and 14. This technique ensures the DATA is present at the latches 13 and 14 before the data is strobed into the latches 13 and 14 ([0019]). Therefore, it is obvious to one of ordinary skill in art to combine the teaching of strobe with delay of Dabral with the

data transfer system of Hirose et al. By doing so, allow DATA to be received first at the receiver. And consequently, provide reliable data communication between two devices.

b) Regarding to claim 3, Dabral disclose wherein said synchro signal is delayed by a half transmission period with respect to the data signal (strob signal is delayed by delay circuit 15 in Fig. 1; the transmission period of strob signal is delayed with respected to DATA signal).

c) Regarding to claim 14, Hirose et al disclose a communication protocol method, comprising:

transmitting (block A in Fig. 1A) along with a data signal (command bus line) a synchronization signal (STRB bus line) indicating to a receiving entity that the data signal comprises new datum (Fig. 1B; Col 1, L60-63); and

inhibiting transmission of the synchronization signal in response to an indication received from the receiving entity of the existence of a congestion condition (BUSY bus line in Fig. 1A; Col 1, L52-59) at the receiving entity (Fig. 1B; Col 1, L63-Col 2, L6; STRB signal stops after the BUSY signal is sent).

Hirose et al disclose all the subject matter above except is silent about whether or not the synchro signal is delayed with respect to the data signal. However, Dabral, in the same field of endeavor, disclose a data transfer system between two devices, wherein the strobe signals are delayed (15 in Fig. 1) before transmitting data to latches 13 and 14. This technique ensures the DATA is present at the latches 13 and 14 before the data is strobed into the latches 13 and 14 ([0019]). Therefore, it is obvious to one of ordinary skill in art to combine the teaching of strobe with delay of Dabral with the

data transfer system of Hirose et al. By doing so, allow DATA to be received first at the receiver. And consequently, provide reliable data communication between two devices.

d) Regarding to claim 15, Hirose et al disclose wherein the data signal is communicated on a first communication line (Command signal line in Fig. 1A) synchronization signal is communicated on a second communication line (STRB signal line in Fig. 1A).

e) Regarding to claim 16, Hirose et al disclose wherein the indication of the existence of a congestion condition at the receiving entity is received over a third communication line (BUSY signal line in Fig. 1A).

f) Regarding to claim 17, Hirose et al disclose including inhibiting transmission of the data signal in response to the indication received from the receiving entity of the existence of a congestion condition at the receiving entity (Fig. 1B; data transmission stops after 5 commands).

g) Regarding to claim 25, Hirose et al disclose a communication system, comprising:

- a first communication block (block A in Fig. 1A);

- a second communication block (block B in Fig. 1A);

- a communication network interconnecting the first and second communication blocks (Fig. 1A); the communication network comprising:

- a first communication line for carrying a data signal (command bus line in Fig. 1A);

a second communication line for carrying a congestion signal (BUSY bus line in Fig. 1A; Col 1, L52-59); and

a third communication line for carrying a synchronization signal (STRB bus line in Fig. 1A); wherein the synchronization signal is active whenever the data signal on the first communication is new datum and inactive whenever the congestion signal on the second communication line is active (Fig. 1B; STRB signal is active as the command signal is new and within process limit, while STRB stops transmitting when BUSY is active after limit of commands has reached).

Hirose et al disclose all the subject matter above except is silent about whether or not the active synchronization signal is delayed with respect to the data signal. However, Dabral, in the same field of endeavor, disclose a data transfer system between two devices, wherein the strobe signals are delayed (15 in Fig. 1) before transmitting data to latches 13 and 14. This technique ensures the DATA is present at the latches 13 and 14 before the data is strobed into the latches 13 and 14 ([0019]). Therefore, it is obvious to one of ordinary skill in art to combine the teaching of strobe with delay of Dabral with the data transfer system of Hirose et al. By doing so, allow DATA to be received first at the receiver. And consequently, provide reliable data communication between two devices.

9. Claims 6, 9, 10, 19, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable by Hirose et al (US 6,917,995) in view of Applicant Admitted Prior Art (AAPA).

a) Regarding to claim 6, Hirose et al disclose a method for synchronizing a data interchange in a semiconductor substrate integrated electronic circuit (IC; abstract) comprising a transmitter block (block A in Fig. 1A) and a receiver block (block B in Fig. 1A) connected through a communication network, comprising:

generating a data signal having a transmission period on a first line that from said transmitter block must be received by the receiver block (command bus line in Fig. 1A);

generating on a second line a congestion signal from the receiver block to the transmitter block when a congestion event (when number of commands reach maximum limit) of the receiver block occurs in order to interrupt the transmission of said data signal (BUSY bus line in Fig. 1A; Col 1, L52-59); and

generating on a third line a synchro signal starting from said transmitter block (STRB bus line in Fig. 1A), this synchro signal indicating to the receiver block that the data signal comprises a new datum (Fig. 1B; Col 1, L60-65), and in that the congestion signal interrupts also the transmission of said synchro signal when a congestion event of the receiver block occurs (Fig. 1B; Col 1, L63-Col 2, L6; STRB signal stops after the BUSY signal is sent).

Hirose et al disclose all the subject matters above except for the specific teaching that the first, second and third communication lines are each comprises a repeater device.

However, AAPA disclose data being transmitted and received through a communication network in a conventional way, wherein tristate repeaters are inserted between each stage of the communication line (B1----Bn in Fig. 1). The tristate type of

repeater device (Bn) on data communication line (5a in Fig. 1), and the congestion communication line (6a) drive the tristate operation of the repeater devices for the data communication line in response to the congestion signal. These repeaters are capable of sampling and maintaining the voltage level of the data signal line being inputted therein ([0016]). Therefore, it is obvious to one of ordinary skill in art to combine the teaching of repeaters in communication line of AAPA with the data transfer system of Hirose et al. By doing so, provide better signal sampling and maintain voltage level of signals.

b) Regarding to claim 9, Hirose et al disclose an integrated electronic circuit being integrated on a semiconductor substrate (IC; abstract) comprising a transmitter block (block A in Fig. 1A) and a receiver block (block B in Fig. 1A) connected through a communication network, said communication network comprising a first line for a data signal (command bus line in Fig. 1A), a second line for a congestion signal (BUSY bus line in Fig. 1A; Col 1, L52-59), and a third line for a synchro signal (Fig. 1B; Col 1, L63-Col 2, L6; STRB signal stops after the BUSY signal is sent).

Hirose et al disclose all the subject matters above except for the specific teaching that the first, second and third communication lines are each comprises a repeater device.

However, AAPA disclose data being transmitted and received through a communication network in a conventional way, wherein tristate repeaters are inserted between each stage of the communication line (B1----Bn in Fig. 1). The tristate type of repeater device (Bn) on data communication line (5a in Fig. 1), and the congestion

communication line (6a) drive the tristate operation of the repeater devices for the data communication line in response to the congestion signal. These repeaters are capable of sampling and maintaining the voltage level of the data signal line being inputted therein ([0016]). Therefore, it is obvious to one of ordinary skill in art to combine the teaching of repeaters in communication line of AAPA with the data transfer system of Hirose et al. By doing so, provide better signal sampling and maintain voltage level of signals.

c) Regarding to claim 10, Hirose et al disclose wherein said signal line comprises a couple of further lines for unidirectional signals indicating the transmission direction between said transmitter block and said receiver block (Fig. 2A and 2C), a negotiation to define the transmission direction being controlled by a further transmission request signal driven by the receiver block (counter 18, controller A, counter 18B, controller B constitutes as negotiator).

d) Regarding to claim 19, Hirose et al disclose a communication system, comprising:

- a first communication block (block A in Fig. 1A);
- a second communication block (block B in Fig. 1A);
- a communication network interconnecting the first and second communication blocks (Fig. 1A); the communication network comprising:
 - a first communication line for carrying a data signal (command bus line in Fig. 1A);

a second communication line for carrying a congestion signal (BUSY bus line in Fig. 1A; Col 1, L52-59); and

a third communication line for carrying a synchronization signal (STRB bus line in Fig. 1A); wherein the synchronization signal is active whenever the data signal on the first communication is new datum and inactive whenever the congestion signal on the second communication line is active (Fig. 1B; STRB signal is active as the command signal is new and within process limit, while STRB stops transmitting when BUSY is active after limit of commands has reached).

Hirose et al disclose all the subject matters above except for the specific teaching that the first, second and third communication line is each split into corresponding stages and comprises a repeater device.

However, AAPA disclose data being transmitted and received through a communication network in a conventional way, wherein tristate repeaters are inserted between each stage of the communication line (B1----Bn in Fig. 1). These repeaters are capable of sampling and maintaining the voltage level of the data signal line being inputted therein ([0016]). Therefore, it is obvious to one of ordinary skill in art to combine the teaching of repeaters in communication line of AAPA with the data transfer system of Hirose et al. By doing so, provide better signal sampling and maintain voltage level of signals.

e) Regarding to claim 21, AAPA disclose tristate type of repeater device (Bn) on data communication line (5a in Fig. 1), and the congestion communication line (6a) drive the tristate operation of the repeater devices for the data communication line in

response to the congestion signal. Therefore, it is obvious to one of ordinary skill in art to implement the tristate repeater device in the additional communication lines for further improve communication system.

11. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable by Applicant Admitted Prior Art (AAPA) in view of Farjad-rad (US 2004/0150453).

a) Regarding to claim 11, AAPA disclose an architecture for manufacturing an integrated electronic circuit being integrated on a semiconductor substrate comprising a transmitter block (2a in Fig. 1) and a receiver block (3a) connected through a communication network, said communication network comprising a plurality of signal lines each split in elementary blocks (A_n), each block being separated through a repeater (B_n), said elementary blocks being connected to said receiver and transmitter blocks through interface devices equipped with unidirectional signals ([0015-0018]).

AAPA disclose all the subject matters above except for the specific teaching that the elementary blocks (A_n) are realized through a multiplexer 2x2.

However, Farjad-rad discloses a phase offset cancellation generator, wherein phase detectors (306a' and 306b' in Fig. 6) are coupled to four switches (402a, 402b, 404a, and 404b respectively). This way minimizes the circuit offset due to mismatch ([0030-0031]). Therefore, it is obvious to one of ordinary skill in art to combine the teaching of phase detectors with switches of Farjad-rad with the communication network of AAPA. By doing so, reduce the effect of phase mismatch and optimize signal synchronization in a communication system.

12. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Farjad-rad (US 2004/0150453), and in further view of Hirose et al (US 6,917,995).

Regarding to claim 12, AAPA and Farjad-rad disclose all the subject matter above except for the specific teaching of unidirectional signals and negotiation for transmitter and receiver.

However, Hirose teaches a communication system between two integrated circuit devices, wherein data and control lines are interposed between microprocessor A and bridge chip B (Fig. 2C). CMD_STRB_A, CMD_STRB_B, Command-A, Command-B, CMD_READY_A, and CMD_READY_B are all unidirectional signals indicating the transmission direction between the transmitter and receiver. Counter 18, controller A, counter 18B, controller B constitutes as negotiator to define the transmission direction being controlled by a further transmission request signal driven by the receiver (Col 4, L43-64). This increases the bus access efficiency even more (Col 6, L56-57).

Therefore, it is obvious to one of ordinary skill in art to combine the teaching of IC communication system of Hirose et al with AAPA. By doing so, provide communication between integrated circuit devices at higher frequencies and more access efficiency of bus lines.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eva Y Zheng whose telephone number is 571-272-3049. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eva Yi Puente
Examiner
Art Unit 2611

November 19, 2007


CHIEH M. FAN
SUPERVISORY PATENT EXAMINER